Midterm Exam

(October 13th @ 5:30 pm)

Presentation and clarity are very important! Show your procedure!

Problem 1 (20 pts)

a) Complete the following table. The decimal numbers are unsigned: (6 pts.)

Decimal	BCD	Binary	Reflective Gray Code
52			
			110011
		1010101	
	000100100010		

b) Complete the following table. Use the fewest number of bits in each case: (12 pts.)

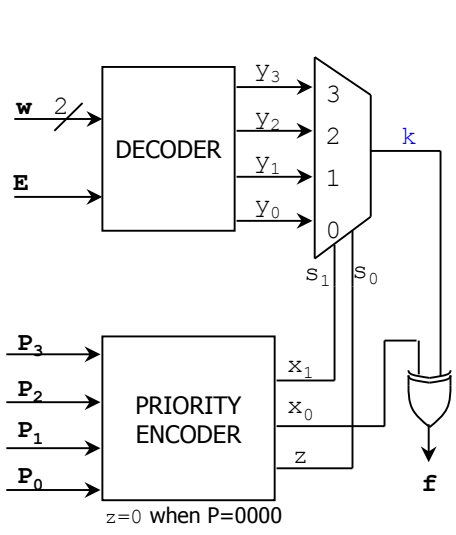
REPRESENTATION			
Decimal	**Sign-and-magnitude**	**1's complement**	**2's complement**
-63			
			100110
		11111	
		01101110	
	1100000		
			10000

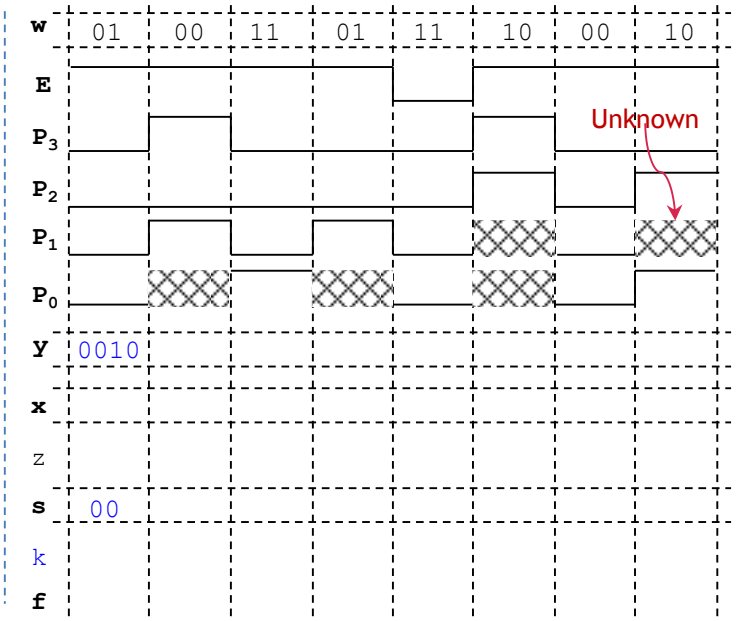
c) Convert the following decimal numbers to their 2's complement representations. (2 pts)

✓ -19.6875 ✓ 16.3125

Problem 2 (15 pts)

- Complete the timing diagram of the circuit shown below. $y = y_3y_2y_1y_0$, $x = x_1x_0$, $s = s_1s_0$





Problem 3 (18 pts)

a) Perform the following additions and subtractions of the following unsigned integers. Use the fewest number of bits n to represent both operators. Indicate every carry (or borrow) from c_0 to c_n (or b_0 to b_n). For the addition, determine whether there is an overflow. For the subtraction, determine whether we need to keep borrowing from a higher byte. (6 pts)

✓ 52 + 17 ✓ 24 - 34

b) Perform the following operations, where numbers are represented in 2's complement. Indicate every carry from c_0 to c_n. For each case, use the fewest number of bits to represent the summands and the result so that overflow is avoided. (8 pts)

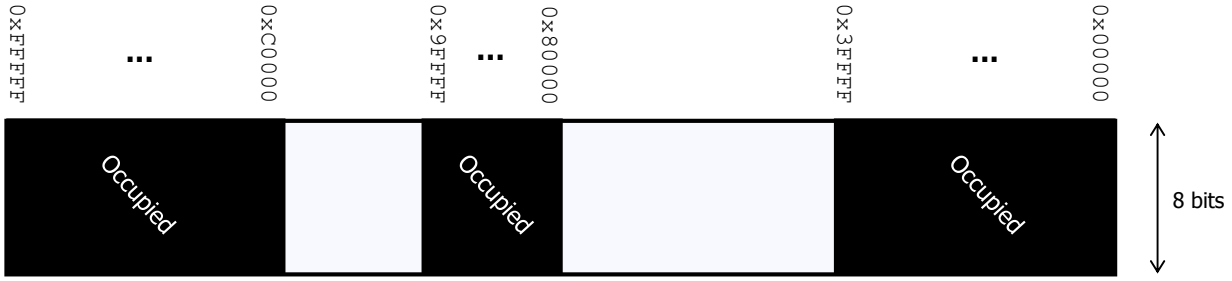
✓ -26 + 45 ✓ -63 - 15

c) Perform binary multiplication of the following numbers that are represented in 2's complement arithmetic with 4 bits. (4 pts)

✓ -7 x 6.

PROBLEM 4 (10 PTS)

- The figure below depicts the entire memory space of a microprocessor. Each memory address occupies one byte. 1KB = 2^{10} bytes, 1MB = 2^{20} bytes, 1GB = 2^{30} bytes
  - ✓ What is the size (in bytes, KB, or MB) of the memory space? What is the address bus size of the microprocessor?
  - ✓ If we have a memory chip of 128 KB, how many bits do we require to address those 128 KB of memory?
  - ✓ We want to connect the 128 KB memory chip to the microprocessor. For optimal implementation, we must place those 128 KB in an address range where every single address shares some MSBs. Provide a list of all the possible address ranges that the 128 KB memory chip can occupy. You can only use any of the non-occupied portions of the memory space as shown below.

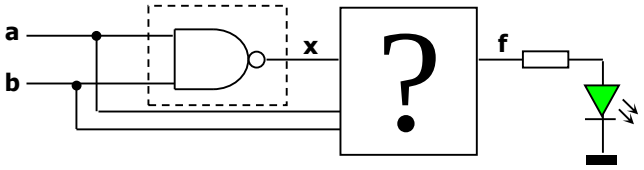


PROBLEM 5 (10 PTS)

- Sketch the circuit that computes $|A - B| \times 4$, where A, B are 4-bit signed (2's complement) numbers. For example: $A = 1010, B = 0111 \rightarrow |A - B| \times 4 = 13 \times 4 = 52$. You can only use full adders and logic gates. Your circuit must avoid overflow.

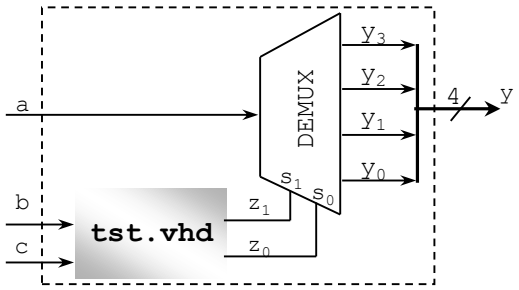
PROBLEM 6 (15 PTS)

- Using only 2-to-1 MUXs, design a circuit that verifies the logical operation of an NAND gate. f='1' (LED ON) if the NAND gate does NOT work properly.
  Assumption: when the NAND gate is not working, it generates 1's instead of 0's and vice versa.



PROBLEM 7 (12 PTS)

- Complete the timing diagram of the following circuit. The VHDL code (`tst.vhd`) corresponds to the shaded circuit.
  $z = z_1 z_0$, $y = y_3 y_2 y_1 y_0$




```
library ieee;
use ieee.std_logic_1164.all;

entity tst is
  port (b,c : in std_logic;
        z: out std_logic_vector(1 downto 0));
end tst;
```

```
architecture bhv of tst is

begin

  process (b, c)
  begin
     z <= c & b;
     if c = '0' then
        z <= "10";
     end if;
  end process;

end bhv;
```